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**ULTRA-THIN FULLY DEPLETED SOI DEVICE AND
METHOD OF FABRICATION**

by

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ULTRA-THIN FULLY DEPLETED SOI DEVICE AND METHOD OF FABRICATION**TECHNICAL FIELD**

The present invention relates generally to semiconductor devices and the fabrication thereof and, more particularly, to a semiconductor device having a thin body region and a high-K gate dielectric.

BACKGROUND

5 A pervasive trend in modern integrated circuit manufacture is to produce semiconductor devices, such as metal oxide semiconductor field effect transistors (MOSFETs), that are as small as possible. In a typical MOSFET, a source and a drain are formed in an active region of a semiconductor layer by implanting N-type or P-type impurities in the layer of semiconductor material. Disposed between the source and the drain is a channel (or body) region. Disposed above the body region is a gate electrode. The gate electrode and the body are spaced apart by a gate dielectric layer. It is noted that MOSFETs can be formed in bulk format (for example, the active region being formed in a silicon substrate) or in a semiconductor-on-insulator (SOI) format (for example, in a silicon film that is
10 disposed on an insulating layer that is, in turn, disposed on a silicon substrate).

15 Although the fabrication of smaller transistors allows more transistors to be placed on a single monolithic substrate for the formation of relatively large circuit systems in a relatively small die area, this downscaling can result in a number of performance degrading effects. For example, in SOI devices with a thin body (e.g.,
20 about 15 nm or less) it may become difficult to adequately control the thickness of the channel.

Accordingly, there exists a need in the art for semiconductor devices, such as MOSFETs, that have enhanced performance and that are made with relatively precise dimensions. There also exists a need for corresponding fabrication
25 techniques to make those semiconductor devices.

SUMMARY OF THE INVENTION

According to one aspect of the invention, the invention is directed to a fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET). The FET includes a layer of semiconductor material disposed over an insulating layer, the insulating layer disposed over a semiconductor substrate. A source and a drain are formed from the layer of semiconductor material. A body is formed from the layer of semiconductor material and disposed between the source and the drain. The layer of semiconductor material is etched such that a thickness of the body is less than a thickness of the source and the drain and such that a recess is formed in the layer of semiconductor material over the body. A gate is formed at least in part in the recess and the gate defining a channel in the body, the gate including a gate electrode spaced apart from the body by a gate dielectric made from a high-K material.

According to another aspect of the invention, the invention is directed to a method of forming a fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET). The method includes providing a layer of semiconductor material, the layer of semiconductor material disposed over an insulating layer, and the insulating layer disposed over a semiconductor substrate; forming a dummy gate on the layer of semiconductor material; doping the layer of semiconductor material to form a source and a drain, and a body region between the source and the drain; removing at least a portion of the dummy gate; etching the layer of semiconductor material to form a recess therein, the recess formed in at least the body region of the layer of semiconductor material such that a thickness of the body is less than a thickness of the source and the drain; and forming a gate at least in part in the recess and the gate defining a channel in the body, the gate including a gate electrode spaced apart from the body by a gate dielectric made from a high-K material.

BRIEF DESCRIPTION OF DRAWINGS

These and further features of the present invention will be apparent with reference to the following description and drawings, wherein:

FIG. 1 is a schematic block diagram of an example semiconductor device formed in accordance with the present invention;

FIG. 2 is a flow chart illustrating a method of forming the semiconductor device of FIG. 1;

FIGs. 3A through 3D illustrate the semiconductor device of FIG. 1 in various stages of manufacture; and

5 FIG. 4 is a schematic block diagram of another example semiconductor device formed in accordance with the present invention

DISCLOSURE OF INVENTION

In the detailed description that follows, identical components have been given the same reference numerals, regardless of whether they are shown in different
10 embodiments of the present invention. To illustrate the present invention in a clear and concise manner, the drawings may not necessarily be to scale and certain features may be shown in somewhat schematic form.

With reference to FIG. 1, a semiconductor device 10 fabricated on a wafer 12 according to an example embodiment of the present invention is illustrated. The
15 illustrated semiconductor device 10 is a fully depleted, semiconductor-on-insulator (SOI), metal oxide semiconductor field effect transistor (MOSFET) used, for example, in the construction of a complimentary metal oxide semiconductor (CMOS) integrated circuit. The semiconductor device 10 has a body 14 having a thickness of less than about 50 Å. In one embodiment, the body 14 has a thickness of about 35
20 Å.

As one skilled in the art will appreciate, the illustrated MOSFET is merely exemplary and the structures and the techniques for fabricating the semiconductor device 10 described herein can be used for other types of semiconductors (e.g., other types of transistors, memory cells, etc.). Although only one semiconductor
25 device 10 is illustrated, one skilled in the art will appreciate that multiple semiconductor devices, of any type (including N-channel devices and P-channel devices), can be formed on the wafer 12.

The semiconductor device 10 is formed using a layer of semiconductor material 16. As illustrated, the layer of semiconductor material 16 can be a
30 semiconductor film (for example, comprised of silicon, silicon-germanium, or the like) that is formed on a layer of insulating material 18 (for example, a buried oxide (BOX))

layer). The insulating layer 18 is, in turn, formed on a semiconductor substrate 20 (also referred to in the art as a handle wafer) so that the resultant devices (e.g., semiconductor device 10) are formed in SOI format.

The semiconductor device 10 includes a source 22 and a drain 24. The body 14 is disposed between the source 22 and the drain 24. The source 22, the drain 24 and the body 24 are formed from the layer of semiconductor material 16 as will be described in greater detail below. In the illustrated embodiment, the body 24 is undoped, but the source 22 and the drain 24 are doped with an appropriate dopant (e.g., N+ doping or P+ doping). Alternatively, the body 14 can be doped as desired. Together, the source 22, the drain 24 and the body 14 form an active region 26. The active region 26 can be defined by isolation regions (not shown), such as shallow trench isolation (STI) regions as is well known in the art.

The source 22 and the drain 24 are relatively thick so as to have low parasitic resistance. In one embodiment, the thickness of the source 22 and the drain 24 is about 400 Å less an amount of semiconductor material consumed by silicidation as discussed below in greater detail. As indicated, the body is relatively thin (e.g., less than about 50 Å). A relatively thin body assists in controlling short channel effects (SCE). SCE generally occur when the gate does not have adequate control over the channel region, and can include threshold voltage (V_t) roll-off, off current (I_{off}) roll-up and drain induced barrier lowering (DIBL). As the physical dimensions decrease, SCE can become more severe. SCE is the result of intrinsic properties of the crystalline materials used in the FET devices. Namely, the band gap and built-in potential at the source/body and drain/body junctions are non-scalable with the reduction of physical device dimensions, such as a reduction in channel length.

A gate 28 is disposed over the body 14 and defines a channel 30 within the body 14 (the channel 30 being interposed between the source 22 and the drain 24 and controlled by a work function of the gate 28). The gate 28 includes a gate electrode 32 spaced apart from the layer of semiconductor material 16 by a gate dielectric 34. As illustrated, the gate 28 is a recessed gate. That is, the layer of semiconductor material 16 has a recess in which the gate 28 is at least partially disposed. The recess is formed by removing a portion of the layer of semiconductor material 16 between the source 22 and the drain 24 such that the body 14 is formed

with a relatively thin thickness (e.g., less than about 50 Å). As illustrated, portions of the source 22 and the drain 24 can also be removed to effectively form extension regions of the source 22 and the drain 24.

The gate electrode 32 can be made from a metal (e.g., tungsten, tantalum, aluminum, nickel, ruthenium, rhodium, palladium, platinum, titanium, molybdenum, etc) or a metal containing compound (e.g., titanium nitride, tantalum nitride, ruthenium oxide, etc.). If desired, a doped semiconductor (e.g., polycrystalline silicon, polycrystalline silicon-germanium, etc.) could also be used for the gate electrode 32. The material of the gate electrode 32 can also be separately selected for N-channel devices and P-channel devices. By way of example, aluminum can be selected for an NMOS device and ruthenium or ruthenium oxide can be selected for PMOS devices.

Disposed adjacent each sidewall of the gate electrode 32 is a spacer 36. The spacers are separated from the gate electrode 32 by the gate dielectric 34. Such a configuration is a result of the spacers 36 being formed prior to the gate dielectric 34. The gate dielectric 34 is formed as a conformal layer over the spacers 36 and the body region 14, which is followed by formation of the gate electrode 32 as will be described in greater detail below. In one embodiment, the spacers 36 are formed from an undoped semiconductor material, such as polycrystalline silicon. Alternatively, the spacers could be formed from an oxide or a nitride.

In one embodiment, the gate dielectric 34 is made from a high-K material or a stack of materials to form a high-K dielectric stack. As used herein, a "high-K material" or a "high-K dielectric material" refers to a material, or stack of materials, having a relative permittivity in one embodiment of about ten (10) or more, and in another embodiment of about twenty (20) or more. Relative permittivity is the ratio of the absolute permittivity (ϵ) found by measuring capacitance of the material to the permittivity of free space (ϵ_0), that is $K = \epsilon/\epsilon_0$. High-K materials will be described in greater detail below. Although other materials can be selected for the gate dielectric 34, hafnium oxide (e.g., HfO_2), zirconium oxide (e.g., ZrO_2), cerium oxide (CeO_2), aluminum oxide (e.g., Al_2O_3), titanium oxide (TiO_2), yttrium oxide (Y_2O_3), barium strontium titanate (BST) are example suitable materials for the gate dielectric 34. In addition, all binary and ternary metal oxides and ferroelectric materials having a K

higher than, in one embodiment, about twenty (20) can be used for the gate dielectric 34.

In an alternative embodiment, the gate dielectric 34 can be made from a standard-K material. As used herein, the term "standard-K material" or "standard-K dielectric material" refers to a dielectric material having a relative permittivity, or K, of up to about ten (10). Example standard-K materials include, for example, silicon dioxide (K of about 3.9), silicon oxynitride (K of about 4 to 8 depending on the relative content of oxygen and nitrogen) and silicon nitride (K of about 6 to 9).

When a high-K material is selected as the gate dielectric 34, the high-K material can have an equivalent oxide thickness (EOT) of about one nanometer (1 nm) or less. In the semiconductor device 10 described herein, a gate dielectric made from a high-K material may be desirable to minimize performance degrading effects, such as leakage, that may occur when the thickness of a standard-K dielectric material becomes thin (e.g., approaching about 1 nm). A high-K dielectric allows for the establishment of a suitable capacitance with a physically thicker dielectric layer. For example, a nitride gate dielectric having a K of about 7.8 and a thickness of about 10 nm is substantially electrically equivalent to an oxide gate dielectric having a K of about 3.9 and a thickness of about 5 nm. In addition, devices fabricated with a high-K dielectric layer tend to have improved reliability.

A relatively thin oxide layer 38 (e.g., silicon oxide) can be disposed between the spacers 36 and the layer of semiconductor material 16. In the illustrated embodiment, the oxide layer 38 is formed between the a source side spacer 36 and the source 22 and the oxide layer 38 is formed between a drain side spacer 36 and the drain 24. These portions can be fabricated in separate processing steps or, as will be described in greater detail below, from one layer of material. In one embodiment, the oxide layer 38 is about 15 Å thick.

When a high-K material is selected as the gate dielectric 34, a buffer interface (not shown) can be used between the layer of semiconductor material 16 and the gate dielectric 34. The buffer interface can be, for example, an oxide layer having a thickness of about 0.5 nm to about 0.7 nm. The buffer interface acts to reduce diffusion and/or penetration of atoms from the high-K dielectric material into the layer of semiconductor material 16 that could lead to a degradation in channel mobility. In

addition, the buffer interface may act to retard reaction of the high-K material with the layer of semiconductor material 16. In one embodiment, the buffer interface can be formed from the same layer of material used to form the oxide layer 38. In this embodiment, a step to remove oxide that is formed between the spacers (discussed below) can be omitted.

In one embodiment, the semiconductor device 10 is provided with a source contact 40 and a drain contact 42. The contacts 40, 42 can be made from a silicide. The silicide can be formed by reacting a metal (such as cobalt) with the layer of semiconductor material 16 to form, for example, CoSi_2 . A tetraethyl-ortho-silicate (TEOS) oxide layer 44 can be formed over the contacts 40, 42. The TEOS oxide layer 44 provides sidewalls to assist in the formation of the spacers 36 as will be described in greater detail below. The TEOS oxide layer 44 can also form a portion of a cap (or passivation) layer. As one skilled in the art will appreciate, the layer 44 can be formed from a material source other than TEOS. Contact holes (not shown), or vias, can be formed in the TEOS oxide layer to establish electrical connectivity to the source contact 40 and the drain contact 42. Other components, such as a gate electrode contact, cap layer, vias, conductor lines and any other appropriate components to interconnect devices formed on the wafer 12, can also be provided.

Referring now to FIG. 2, a method 50 of forming the semiconductor device 10 is illustrated. With additional reference to FIG. 3A, the method 50 starts in step 52 where the layer of semiconductor material 16 is provided. As indicated above, the layer of semiconductor material 16 can be a semiconductor film (such as a silicon film or a silicon-germanium film) formed as part of a SOI substrate stack. In such an arrangement, the layer of semiconductor material 16 is formed on the insulating layer 18, which is formed on the semiconductor substrate 20. In one embodiment, the layer of semiconductor material 16 can have a thickness of about 400 Å. The thickness of the layer of semiconductor material 16 will be selectively reduced to form the body region 14 as described below in greater detail. In one embodiment, the insulating layer 18 can have a thickness of about 500 Å.

If desired, isolation regions (not shown) can be formed in the layer of semiconductor material 16 to define the size and placement of multiple active

regions 26 on the wafer 12. The formation of isolation regions, such as STI regions, are well known in the art and will not be described in greater detail.

Next, in step 54, a dummy gate 56 can be formed on the layer of semiconductor material 16. The dummy gate 56 can be made from, for example, a nitride (e.g., silicon nitride). However, one skilled in the art will appreciate that any other appropriate material can be selected for the dummy gate 56. The dummy gate 56 can also be separated from the layer of semiconductor material 16 by an oxide layer 57, or a layer of other suitable material. The oxide layer 57 assists in matching material properties, such as stress parameters, between the dummy gate 57 and the layer of semiconductor material 16 during, for example, high temperature processing. The dummy gate 56 can be formed by convention processing, such as growing or depositing a layer of the desired material(s) and patterning the layer(s) with an appropriate technique, such as photolithography.

Next, in step 58, the source 22 and the drain 24 can be doped by implanting an appropriate dopant species. Briefly, for a P-type source/drain, ions such as boron, gallium or indium can be implanted. For an N-type source/drain, ions such as antimony, phosphorous or arsenic can be implanted. In one embodiment of the invention, the semiconductor device 10 is configured as an N-channel device and the source 22 and the drain 24 are implanted with phosphorous with an energy of about 5 keV to 10 keV and a dose of about 2×10^{15} atoms/cm² to about 4×10^{15} atoms/cm². The ions used to form the source 22 and the drain 24 may diffuse under the dummy gate 56 is conventional. Following source/drain ion implantation, the wafer 12 can be annealed to activate the dopant species. For example, in the forgoing example where phosphorous has been implanted, the wafer 12 can be annealed at about 1000°C for about 10 seconds.

With additional reference to FIG. 3B, the method 50 continues in step 60 where the source contact 40 and the drain contact 42 are formed. In the illustrated embodiment, the source contact 40 and the drain contact are formed from silicide. Briefly, the silicide can be formed by depositing a layer of metal (such as cobalt, nickel, molybdenum or titanium) and reacting the metal with the layer of semiconductor material 16.

Thereafter, in step 62, the layer 44 can be formed. The layer 44 can be, for example, an oxide using TEOS as a material source as is known in the art. The layer 44 can be formed by depositing a layer of the desired material and polishing the deposited layer (using, for example, chemical mechanical planarization (CMP))

5 to remove undesired material from on top of the dummy gate 56.

Next, in step 64 and with additional reference to FIG. 3C, the dummy gate 56 is removed. In the illustrated embodiment, the dummy gate 56 is formed from a nitride and the dummy gate 56 can be removed using a hot phosphoric acid etch.

Should the dummy gate 56 include the underlying oxide layer 57, the oxide layer 57
10 can also be removed using an appropriate etch technique.

Thereafter, in step 66, the layer of semiconductor material 16 is etched to form a recess 68 in which the gate 28 will be formed as described below in greater detail. In the illustrated embodiment where the layer of semiconductor material 16 is formed from silicon, the layer of semiconductor material 16 can be etched with
15 ammonium hydroxide (e.g., NH_4OH). The layer of semiconductor material 16 is etched for a duration of time so that about 50 Å to about 65 Å of semiconductor material remains over the isolating layer 18. The amount of remaining semiconductor material will depend on the desired end thickness of the body region 14 following the completion of subsequent processing steps described below that
20 may consume additional portions of the semiconductor material from the layer of semiconductor material 16. In the illustrated embodiment, the layer of semiconductor material 16 has an initial thickness of about 400Å. Therefore, in the illustrated embodiment, about 350 Å of semiconductor material can be removed from the layer of semiconductor material 16.

25 Next, in step 70, the layer of semiconductor material 16 is oxidized to form the oxide layer 38. The oxide layer 38 is formed from exposed portions of the layer of semiconductor material 16 and extends from the source contact 40 to the drain contact 42. One reason for oxidizing the etched surface of the layer of semiconductor material 16 is to reduce the number of defects that may be caused
30 by etching of the layer of semiconductor material 16.

In the illustrated embodiment, the oxide layer 38 can be about 15 Å thick. The oxide layer 38 can be formed, for example, by exposing the wafer to heat (e.g.,

about 600°C to about 800°C) in an oxygen containing atmosphere. Should the oxide layer 38 also be used as a buffer interface for the subsequently formed high-K gate dielectric 34, the oxide layer 38 can be formed to be thinner than 15 Å.

With additional reference to FIG. 3D, the method 50 continues in step 72

5 where the spacers 36 are formed. The spacers 36 can be formed by depositing a layer of desired material to a thickness of about 200 Å to about 300 Å or, alternatively, to overfill the recess 68. In either case, such a deposited layer can conform to side walls of the layer 44. In the illustrated embodiment, the material used for the spacers 36 is an undoped polycrystalline semiconductor, such as
10 polycrystalline silicon (often referred to in the art as polysilicon or simply poly). The deposited material can then be polished to have an upper surface generally even with the upper surface of the TEOS oxide layer 44. Next, the material can be anisotropically etched back to the underlying layer, which is the oxide layer 38 in the illustrated embodiment. It is noted that the spacers 36 are formed adjacent
15 sidewalls of the layer 44. The sidewalls of the layer 44 were exposed when the dummy gate 56 (FIG. 3B) was removed.

Thereafter, in step 74, a portion of the oxide layer 38 formed between the spacers 36 can be removed, such as by wet chemical etching. Accordingly, the oxide layer 38 can be considered to be a sacrificial layer. The resulting thickness of
20 the body 14 will enable the semiconductor device 10 to be fully depleted.

It is noted that the portion of the oxide layer 28 can alternatively be kept in place to serve as a buffer interface for the gate dielectric 34. In yet another alternative embodiment, the oxide layer 38 can be removed between the spacers 38 and replaced by another desired layer, including another oxide layer. The formation
25 of another oxide layer can be used, for example, to finely tune the thickness of the body 14 and/or to form a buffer interface. In one example, the layer of semiconductor material 16 can be oxidized to consume additional semiconductor material, such as by a low temperature (about 500°C) thermal oxidation process. In another example, oxide material can be deposited, such as by a remote plasma
30 deposition process, an atomic layer deposition (ALD) process or the like. A deposited layer, in most circumstances, would be formed as a conformal layer such that oxide would also be formed on an upper surface of the layer 44 (such oxide

could be polished off if desired) and over the spacer 36 (such oxide could be left in place).

Next, in step 76, a layer of high-K material 78 can be formed. The layer of high-K material 78 is used to form the gate dielectric 34. The layer of high-K

5 material 78 can be deposited as a conformal layer over the layer 44, the spacers 36 and the exposed portion of the layer of semiconductor material 16 between the spacers 36 (or, if present, over a buffer interface formed between the spacers 36).

Exemplary high-K materials are identified below in Table 1. It is noted that Table 1 is not an exhaustive list of high-K materials and other high-K materials may be

10 available.

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TABLE 1

Dielectric Material	Approximate Relative Permittivity (K)
aluminum oxide (Al_2O_3)	9-10
zirconium silicate	12
hafnium silicate	15
hafnium silicon oxynitride	16
hafnium silicon nitride	18
lanthanum oxide (La_2O_3)	20-30
hafnium oxide (HfO_2)	40
zirconium oxide (ZrO_2)	25
cerium oxide (CeO_2)	26
bismuth silicon oxide ($\text{Bi}_4\text{Si}_2\text{O}_{12}$)	35-75
titanium dioxide (TiO_2)	30
tantalum oxide (Ta_2O_5)	26
tungsten oxide (WO_3)	42
yttrium oxide (Y_2O_3)	20
lanthanum aluminum oxide (LaAlO_3)	25
barium strontium titanate ($\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$)	~20 - ~200
barium strontium oxide ($\text{Ba}_{1-x}\text{Sr}_x\text{O}_3$)	~20 - ~200
PbTiO_3	~20 - ~200
barium titanate (BaTiO_3)	~20 - ~200
strontium titanate SrTiO_3	~20 - ~200
PbZrO_3	~20 - ~200
PST ($\text{PbSc}_x\text{Ta}_{1-x}\text{O}_3$)	3000
PZN ($\text{PbZn}_x\text{Nb}_{1-x}\text{O}_3$)	~500 - ~5000
PZT ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$)	~150 - ~1000
PMN ($\text{PbMg}_x\text{Nb}_{1-x}\text{O}_3$)	~500 - ~5000

It is noted that the K-values for both standard-K and high-K materials may vary to some degree depending on the exact nature of the dielectric material. Thus, for example, differences in purity, crystallinity and stoichiometry, may give rise to variations in the exact K-value determined for any particular dielectric material.

As used herein, when a material is referred to by a specific chemical name or formula, the material may include non-stoichiometric variations of the stoichiometrically exact formula identified by the chemical name. For example, tantalum oxide, when stoichiometrically exact, has the chemical formula Ta_2O_5 , but
 5 may include variants of stoichiometric Ta_2O_5 , which may be referred to as Ta_xO_y , in which either of x or y vary by a small amount. For example, in one embodiment, x may vary from about 1.5 to 2.5, and y may vary from about 4.5 to about 5.5. In another embodiment, x may vary from about 1.75 to 2.25, and y may vary from about 4 to about 6. Such variations from the exact stoichiometric formula fall within
 10 the definition of tantalum oxide. Similar variations from exact stoichiometry for all chemical names or formulas used herein are intended to fall within the scope of the present invention. For example, again using tantalum oxide, when the formula Ta_2O_5 is used, Ta_xO_y is included within the meaning. Thus, in the present disclosure, exact stoichiometry is intended only when such is explicitly so stated. As
 15 will be understood by those of skill in the art, such variations may occur naturally, or may be sought and controlled by selection and control of the conditions under which materials are formed.

With continued reference to FIGS. 2 and 3D, the method 50 continues in step
 80 where a layer of gate electrode material 82 is formed over the layer of high-K
 20 material 78. The gate electrode material 82 can be deposited by chemical vapor deposition (CVD) to a thickness of about 250 Å. The use of CVD to deposit the layer of gate electrode material 82 is advantageous to minimize the introduction of additional interface charge.

As illustrated, the resulting layer of gate electrode material 82 may be formed
 25 with a notch. This notch can optionally be filled with an appropriate material, such as a metal (for example, tungsten). Alternatively, the recess 68 (FIG. 3C) can be overfilled with gate electrode material to avoid formation of the notch.

As indicated above, the layer of gate electrode material 82 can be composed
 of a metal (e.g., tungsten, tantalum, aluminum, nickel, ruthenium, rhodium,
 30 palladium, platinum, titanium, molybdenum, etc) or a metal containing compound (e.g., titanium nitride, tantalum nitride, ruthenium oxide, etc.). If desired, a semiconductor (e.g., polycrystalline silicon, polycrystalline silicon-germanium, etc.)

could also be used. The gate electrode material layer 82 can be selected for N-channel devices (e.g., aluminum) or for P-channel devices (e.g., ruthenium or ruthenium oxide).

Thereafter, in step 84 and with additional reference to FIG. 1, the layer of gate electrode material 82 and the layer of high-K material 78 can be polished (using, for example, CMP) to remove portions of the layer of gate electrode material 82 and the layer of high-K material 78 that are disposed over the layer 44.

The method 50 can continue in step 86 where any additional process to complete the formation of the semiconductor device 10 and to interconnect devices formed on the wafer 12 can be carried out. Such additional processing can include steps to form, for example, a cap layer, contact holes or vias, conductor runs and so forth.

The method 50 shows a specific order of steps for fabricating the semiconductor device 10. However, it is understood that the order may differ from that depicted. For example, the order of two or more steps may be altered relative to the order shown. Also, two or more steps may be carried out concurrently or with partial concurrence. In addition, various steps may be omitted and other steps may be added. Furthermore, the method 50 can be modified for the formation of devices other than the illustrated MOSFET. It is understood that all such variations are within the scope of the present invention.

With reference to FIG. 4, an alternative embodiment of the semiconductor device 10 (FIG. 1) is illustrated. It is noted that in FIG. 4, components of the semiconductor device 10' have been given the same reference numerals as counterpart components of the semiconductor device 10 illustrated in FIG. 1, but with a prime symbol (') added thereto. The semiconductor device 10' is made by variations to the method 50 where the spacers 36' are formed from the dummy gate 56 (FIGS. 3A and 3B) material and the layer of semiconductor material 16' is etched using a modified technique than that described in step 66 of method 50. One skilled in the art will appreciate that the modifications to the method 50 described below relate to modifications of steps 64 to 74. One skilled in the art will also appreciate that not all of the modifications to the method 50 described below need to be carried out together. For example, the spacers 36' can be formed using the modified

technique and the etching of the layer of semiconductor material 16' can remain as described in method 50, or vice-versa.

As indicated, the spacers 36' are made from material of the dummy gate 56 and, if present, material of the oxide layer 57 disposed under the dummy gate 56.

- 5 Formation of the spacers 36' from the material of the dummy gate 56/oxide layer 57 can be accomplished by modifying step 64. For example, using reactive ion etching (RIE) the dummy gate 56 and oxide layer 57 can be anisotropically etched to form the spacers 36'. Thus, in the modified example, step 72 can be omitted.

As indicated, the techniques used to form the recess in the layer of

- 10 semiconductor material 16' can also be modified. Upon removal of the dummy gate 56 and oxide layer 57, or upon removal of a portion of the dummy gate 56 and oxide layer 57 to form the spacers 36', the layer of semiconductor material 16 can be anisotropically etched (using, for example, RIE) to reduce the thickness of the layer of semiconductor material 16'. For example, if the layer of semiconductor material 15 16' has a beginning thickness of about 400 Å, then about 250 Å to about 300 Å of semiconductor material can be removed using RIE. Thereafter, wet etching (using, for example, ammonium hydroxide) can be used to remove an additional amount of semiconductor material (for example, about 30 Å to about 50 Å). Thereafter, the layer of semiconductor material can be oxidized to form an oxide layer and to 20 consume an additional amount of semiconductor material. The oxide layer is sacrificial and can be removed. In one embodiment, enough semiconductor material can be oxidized such that about 35 Å to about 50 Å of semiconductor material is left in place over the isolating layer 18' for use as the body 14'/channel 30'. Without intending to be bound by theory, the foregoing method of forming the recess in the 25 layer of semiconductor material 16' will assist in establishing a suitable interface between the gate dielectric 34' and the layer of semiconductor material 16'. However, if desired, an oxide buffer interface can be used between the gate dielectric 34' and the layer of semiconductor material 16'.

- 30 Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes all changes, modifications and equivalents coming within the spirit and terms of the claims appended hereto.